Claims

[c1] 1. A multiple-gate transistor comprising:

a channel region;

a logic gate adjacent a first side of said channel region;

a floating gate adjacent a second side of said channel region, wherein said first side is opposite said second side; and

a programming gate adjacent said floating gate, wherein said floating gate is between said programming gate and said channel region.

[c2] 2. The transistor in claim 1, further comprising a gate oxide between said channel region and said logic gate and a first insulator between said channel region and said floating gate, wherein said first insulator is thicker than said gate oxide.

[c3] 3. The transistor in claim 1, wherein voltage in said logic gate causes said transistor to switch on and off.

[c4] 4. The transistor in claim 1, wherein charge in said floating gate adjusts the threshold voltage of said transistor.

[c5] 5. The transistor in claim 1, wherein said transistor comprises a fin-type field effect transistor (FinFET).

[c6] 6. The transistor in claim 1, further comprising source and drain regions at ends of said channel region, wherein said channel region comprises the middle portion of a fin structure and said source and drain regions comprise end portions of said fin structure.

[c7] 7. The transistor in claim 1, wherein said floating gate is electrically insulated from other structures.

[c8] 8. A multiple-gate transistor comprising:

a channel region;

source and drain regions at ends of said channel region;

a gate oxide on a first side of said channel region;

a logic gate adjacent said first gate oxide, wherein said gate oxide is between said logic gate and said channel region;

a first insulator on a second side of said channel region, wherein said second side of said channel region is opposite said first side;

a floating gate adjacent said first insulator, wherein said first insulator is between said floating gate and said channel region;

a second insulator adjacent said floating gate; and

a programming gate adjacent said second insulator, wherein said second insulator is between said programming gate and said floating gate.

[c9] 9. The transistor in claim 8, wherein said first insulator is thicker than said gate oxide.

[c10] 10. The transistor in claim 8, wherein voltage in said logic gate causes said transistor to switch on and off.

[c11] 11. The transistor in claim 8, wherein charge in said floating gate adjusts the threshold voltage of said transistor.

[c12] 12. The transistor in claim 8, wherein said transistor comprises a fin-type field effect transistor (FinFET).

[c13] 13. The transistor in claim 8, wherein said channel region comprises the middle portion of a fin structure and said source and drain regions comprise end portions of said fin structure.

[c14] 14. The transistor in claim 8, wherein said floating gate is electrically

insulated from other structures.

[c15] 15. A method of manufacturing a multiple-gate transistor, said method comprising:
forming a channel region;
forming a logic gate adjacent a first side of said channel region;
forming a floating gate adjacent a second side of said channel region, wherein said first side is opposite said second side; and
forming a programming gate adjacent said floating gate, wherein said floating gate is between said programming gate and said channel region.

[c16] 16. The method in claim 15, further comprising forming a gate oxide between said channel region and said logic gate and forming a first insulator between said channel region and said floating gate, wherein said first insulator is thicker than said gate oxide.

[c17] 17. The method in claim 15, wherein voltage in said logic gate causes said transistor to switch on and off.

[c18] 18. The method in claim 15, wherein charge in said floating gate adjusts the threshold voltage of said transistor.

[c19] 19. The method in claim 15, wherein said transistor comprises a fin-type field effect transistor (FinFET).

[c20] 20. The method in claim 15, further comprising source and drain regions at ends of said channel region, wherein said channel region comprises the middle portion of a fin structure and said source and drain regions comprise end portions of said fin structure.

[c21] 21. The method in claim 15, wherein said floating gate is electrically insulated from other structures.

[c22] 22. A method of manufacturing a multiple-gate transistor, said method comprising:

forming a channel region;

forming source and drain regions at ends of said channel region;

forming a gate oxide on a first side of said channel region;

forming a logic gate adjacent said first gate oxide, wherein said gate oxide is between said logic gate and said channel region;

forming a first insulator on a second side of said channel region, wherein said second side of said channel region is opposite said first side;

forming a floating gate adjacent said first insulator, wherein said first insulator is between said floating gate and said channel region;

forming a second insulator adjacent said floating gate; and

forming a programming gate adjacent said second insulator, wherein said second insulator is between said programming gate and said floating gate.

[c23] 23. The method in claim 22, wherein said first insulator is thicker than said gate oxide.

[c24] 24. The method in claim 22, wherein voltage in said logic gate causes said transistor to switch on and off.

[c25] 25. The method in claim 22, wherein charge in said floating gate adjusts the threshold voltage of said transistor.

[c26] 26. The method in claim 22, wherein said transistor comprises a fin-type field effect transistor (FinFET).

[c27] 27. The method in claim 22, wherein said channel region comprises the middle portion of a fin structure and said source and drain regions comprise end portions of said fin structure.

[c28] 28. The method in claim 22, wherein said floating gate is electrically insulated from other structures.